PATENT ABSTRACTS OF JAPAN

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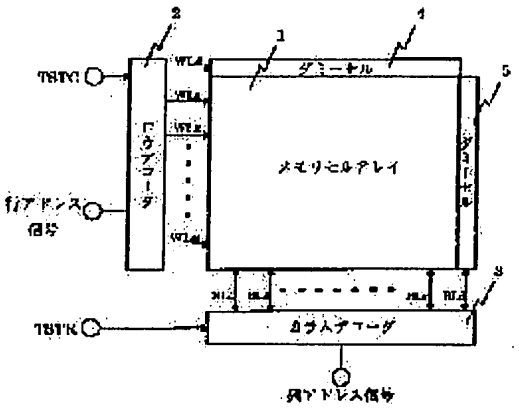
(54) SEMICONDUCTOR MEMORY

(57)Abstract:
PROBLEM TO BE SOLVED: To shorten the test time and to reduce the chip cost by providing a dummy memory cell in which an internal memory value is fixed outside a memory cell being remotest from decoders of word lines and bit lines of an address signal, and enabling a test of word lines and bit lines to be performed by only reading successively data of a dummy memory cell at the time of a test.
SOLUTION: When a bit line is tested, a row decoder 2 prohibits decoding operation of a row address signal by a test signal TSTC and starts a word line WLD connected to a dummy cell 4 in a timing being the same as that of a normal word line. A column address signal is varied in this state, bit line is successively selected, data of the dummy cell 4 is read out (n) times, verified with an internal memory value in the dummy cell 4 previously set, and a test is performed. In the same way, a word test is performed. Thus, as a simple test is performed by selecting simply and successively word lines and bit lines, a test can be performed in a short time.



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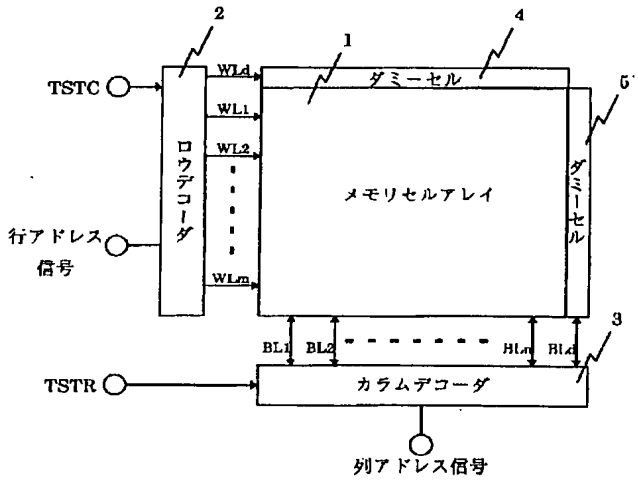
(54)【発明の名称】　半導体記憶装置

(57)【要約】
【課題】試験時間が短く、周辺回路からのノイズに強い半導体記憶装置を提供する。
【解決手段】ワード線およびビット線のデコーダから最も遠いメモリセルの外側に内部記憶値が固定されたダミーのメモリセルを配置する。
【効果】固定されたダミーセルのデータを順次読み込むだけでワード線およびビット線の試験が可能となる。また、ダミーセルを従来の形状ダミーを配置する場所に配置したのでチップ面積が大きくなることもなく、周辺回路からのノイズを受けにくいメモリセルを提供できる。



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【特許請求の範囲】

【請求項１】外部から入力されるアドレス信号がデコードされて選択される複数のワード線およびビット線と、該各ワード線と各ビット線の交差個所に設けられたメモリセルを具備し、前記アドレス信号のワード線およびビット線のデコーダから最も遠いメモリセルの外側に内部記憶値が固定されたダミーのメモリセルを具備することを特徴とした半導体記憶装置。

【請求項２】請求項１記載のダミーのメモリセルは試験手段により選択される相補のビット線対に接続され、外部から入力されるアドレス信号がデコードされて選択されるワード線に接続されることを特徴とした半導体記憶装置。

【請求項３】請求項１記載のダミーのメモリセルは試験手段により選択されるワード線に接続され、伝送トランジスタが外部から入力されるアドレス信号がデコードされて選択される相補のビット線に接続されることを特徴とした半導体記憶装置。

【請求項４】前記ダミーのメモリセルには一方のビット線にソースまたはドレインが接続され、ゲートには外部から入力されるアドレス信号がデコードされて選択されるワード線または試験時に選択されるワード線が接続される伝送トランジスタを設け、該伝送トランジスタのビット線に接続される端子とは逆側の端子が第一の電源電圧に固定されており、もう一方のビット線には同様の構成で伝送トランジスタのビット線に接続される端子とは逆側の端子が第二の電源電圧に固定されていることを特徴とした半導体記憶装置。

【請求項５】前記ダミーのメモリセルを構成するトランジスタは単一導電型であり同一ウェル領域に配置され、該ウェル領域はメモリセルアレイの周囲を連続して取り囲むことを特徴とした半導体記憶装置。

【発明の詳細な説明】

【０００１】

【発明の属する技術分野】本発明は半導体記憶装置に関し、特にワード線およびビット線の簡易試験に関する。

【０００２】

【従来の技術】従来の半導体記憶装置は、図２のメモリセル周辺のブロック図に示されるように、外部から入力されたアドレス信号がプリデコードされた信号が行アドレス信号としてロウデコーダ２に入力され、該ロウデコーダはさらに行アドレス信号をデコードしてｍ本のワード線ＷＬ１からＷＬｍの内の１本を選択する。一方同様に外部から入力されたアドレス信号がプリデコードされた列アドレス信号を入力としたカラムデコーダ３はｎ本のビット線ＢＬ１からＢＬｎの内の１本を選択する。ビット線は２本１組の相補のデータ線である場合もあるが、簡単のため１本のみ表示している。図２に示される半導体記憶装置のメモリセル周りの構成は、書き込み／読み出し可能なＲＡＭ（Ｒａｎｄｏｍ　Ａｃｃｅｓｓ

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Ｍｅｍｏｒｙ）でも読み出し専用のＲＯＭ（Ｒｅａｄ　Ｏｎｌｙ　Ｍｅｍｏｒｙ）でも同じである。図２に示される半導体記憶装置の動作試験を行うためには、１本のワード線を選択すると同時に１本（１対）のビット線を選択し、データを読み書きして入出力データの照合をとることで行われる。ＲＯＭの場合はデータをメモリセルアレイの数ｍ×ｎ回読み出して期待値と照合するのみでよいが、ＲＡＭの場合はデータを一旦書き込んだ後に、書き込んだデータを読み出してデータの照合を行うので、単純に考えてＲＯＭの２倍程度の試験時間がかかってしまう。また近年の半導体プロセスの微細化に伴ってメモリ容量も増大の一路をたどり、それに伴い半導体装置の試験時間にも膨大な時間を割かなければならなくなったので、半導体装置のコストアップにも繋がってしまう。

【０００３】

【発明が解決しようとする課題】半導体装置は通常ウェハーの状態で全メモリセルに対して試験を行い、モールド品などにパッケージされてからも同様の試験が行われる。そのための試験時間が半導体装置のコストに直接跳ね返ってしまう。そこで、試験時間の短縮が必要なのであるが、従来の方法では全メモリセルに対して試験を行わなければならず、試験時間の短縮化を図ることができないという欠点がある。

【０００４】

【課題を解決するための手段】外部から入力されるアドレス信号がデコードされて選択される複数のワード線およびビット線と、該各ワード線と各ビット線の交差個所に設けられたメモリセルを具備し、前記アドレス信号のワード線およびビット線のデコーダから最も遠いメモリセルの外側に内部記憶値が固定されたダミーのメモリセルを具備することを特徴としている。

【０００５】

【発明の実施の形態】次に、本発明について図面を参照して説明する。図１は本発明の一実施例におけるメモリセル周辺のブロック図である。図中１はｍ行ｎ列のマトリクス状に配置されたメモリセルのアレイ、２はワード線を選択するロウデコーダ、３はビット線を選択するカラムデコーダ、４および５は内部記憶値が固定されたダミーのメモリセルである。通常動作において半導体装置外部より入力されたアドレス信号はアドレス入力回路を経て、必要に応じてプリデコードされた後ロウデコーダ２に行アドレス信号として入力される。ロウデコーダはこれを受けてさらにデコード動作を行い、ｍ本のワード線ＷＬ１からＷＬｍの内から１本のワード線のみを選択する。同様に外部より入力されたアドレス信号はアドレス入力回路を経て、必要に応じてプリデコードされた後カラムデコーダ３に列アドレス信号として入力され、カラムデコーダはさらにデコード動作を行い、ｎ本（ｎ対）のビット線ＢＬ１からＢＬｎの内の１本（１対）を

選択することにより、選択されたワード線とビット線の交点に存在するメモリセルがアクティブになり、メモリセルに対して読み出しおよび書き込みが可能になる。以上の動作は従来の半導体記憶装置と変わりない。次に半導体の試験をする時には半導体装置外部よりテスト信号が入力されて、ビット線を試験するときは試験信号ＴＳＴＣがロウデコーダ２に入力され、ロウデコーダは行アドレス信号のデコード動作を禁止してダミーセル４に接続されているワード線ＷＬｄを通常のワード線と同じタイミングで立ち上げる。この状態で列アドレス信号を変化させてビット線を順次選択してダミーのメモリセルのデータをｎ回読み出し、予め設定されているダミーのメモリセルの内部記憶値と照合して試験を行う。同様に、ワード線を試験するときには試験信号ＴＳＴＲがカラムデコーダ３に入力されるため、カラムデコーダは列アドレス信号のデコード動作を禁止してダミーセル５に接続されているビット線ＢＬｄを通常のビット線と同じタイミングで選択する。この状態で行アドレス信号を変化させてワード線を順次選択してダミーのメモリセルのデータをｍ回読み出し、予め設定されているダミーのメモリセルの内部記憶値と照合して試験を行う。このようにしてワード線およびビット線を順次単一選択することにより簡易試験を行うので（ｍ＋ｎ）回ダミーセルのデータを読み出すという短時間の試験が可能になる。

【０００６】図３は図１におけるメモリセルアレイとダミーセルの回路図の一部を示したものである。波線で囲まれたメモリセル１１から１４は各２個のＮチャネル型トランジスタで構成される伝送トランジスタおよび駆動トランジスタと、２個のＰチャネル型トランジスタで構成される負荷トランジスタからなる完全ＣＭＯＳ型のメモリセルである。図では完全ＣＭＯＳ型のメモリセルを用いているが、負荷トランジスタがＴＦＴであるものでも、高抵抗型のものでも構わない。４１から４４はゲートをビット線の試験時に選択されるワード線ＷＬｄに接続されたＮチャネル型トランジスタであり、ドレインまたはソースが相補のビット線対ＸＢＬｎ－１／ＢＬｎ－１およびＸＢＬｎ／ＢＬｎに接続され、もう一方の端子が電源電位あるいは接地電位に接続されたダミーセルである。５１から５４はゲートを通常動作時に選択されるワード線に接続されたＮチャネル型トランジスタであり、ドレインまたはソースが試験時に選択される相補のビット線対ＸＢＬｄ／ＢＬｎｄに接続され、もう一方の端子が電源電位あるいは接地電位に接続されたダミーセルである。図３を使ってまず通常の動作を説明する。半導体装置外部より入力されたアドレス信号はアドレス入力回路を経て、必要に応じてプリデコードされた後ロウデコーダに行アドレス信号として入力され、ロウデコーダはこれを受けてさらにデコード動作を行い、ｍ本のワード線ＷＬ１からＷＬｍの内から１本のワード線が選択され論理レベルが“Ｈ”になり、このワード線に接続されているメモリセルの伝送トランジスタがＯＮする。同様に外部より入力されたアドレス信号はアドレス入力回路を経て、必要に応じてプリデコードされた後カラムデコーダに列アドレス信号として入力され、カラムデコーダはさらにデコード動作を行い、ｎ対のビット線ＸＢＬ１／ＢＬ１からＸＢＬｎ／ＢＬｎの内の１対を選択することにより、選択されたワード線とビット線の交点に存在するメモリセルがアクティブになり、メモリセルに対して読み出しおよび書き込みが可能になる。例えば、ワード線ＷＬ１およびビット線ＸＢＬｎ－１／ＢＬｎ－１が選択されると、メモリセル１１に対してアクセスが可能になり、図には表示していないがデータを読み出すときにはメモリセルの記憶ノードの電位差が伝送トランジスタを介してビット線対に現れ、この微少な電位差をセンスアンプにて増幅する。ＸＢＬｎ－１に伝送トランジスタを介して接続されたメモリセルの記憶ノードが“Ｈ”レベル、逆側のノードが“Ｌ”レベルであれば、ＢＬｎ－１にはＸＢＬｎ－１より低い電位が現れ該当するメモリセルには“０”データが保持されていることになる。逆にＸＢＬｎ－１に伝送トランジスタを介して接続されたメモリセルの記憶ノードが“Ｌ”レベル、逆側のノードが“Ｈ”レベルであれば該当するメモリセルには“１”データが保持されていることになる。データの書き込み時には選択されたビット線に接続されているライトバッファから大きい電位差のついた電位がビット線対に与えられ、伝送トランジスタを介してメモリセルに論理データとして書き込まれる。すなわちメモリセルに“０”データを書き込むにはＢＬｎ－１に“Ｈ”レベル、ＸＢＬｎ－１には“Ｌ”レベルの電位を与え、“１”を書き込みたいときにはその逆の電位を与える。従来の半導体記憶装置は試験時において、このような動作により特定のパターンのデータをメモリセルに書き込み、メモリセルからデータを読み出すことにより試験装置内でデータの照合をとり、半導体記憶装置の良否を判断している。しかし本発明の一実施例である図３のダミーのメモリセルを用いればデータを書き込む必要がない。まずビット線を試験するときはダミーのワード線ＷＬｄのみを通常のワード線と同じタイミングで選択して“Ｈ”レベルに立ち上げる。次に外部から与えられる列アドレス信号を変化させてることによりビット線をＸＢＬ１／ＢＬ１からＸＢＬｎ／ＢＬｎまで順次選択してダミーのメモリセルのデータをｎ回読み出し、予め設定されているダミーのメモリセルの内部記憶値と照合して試験を行う。同様に、ワード線を試験するときにはダミーのビット線ＸＢＬｄ／ＢＬｄを通常のビット線と同じタイミングで選択する。この状態で外部から与えられる行アドレス信号を変化させてワード線をＷＬ１からＷＬｍまで順次選択してダミーのメモリセルのデータをｍ回読み出し、予め設定されているダミーのメモリセルの内部記憶値と照合して試験を行う。すなわちビット線試験時

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にビット線ショートなどの不良がない限りＸＢＬｎ－１／ＢＬｎ－１、ＸＢＬｎ／ＢＬｎが順次選択されるとＸＢＬｎ－１には“Ｌ”レベルの電位、ＢＬｎ－１には“Ｈ”レベルの電位が現れるので“１”データが読み出され、ＸＢＬｎには“Ｈ”レベルの電位、ＢＬｎには“Ｌ”レベルの電位が現れるので“０”データが読み出されることになる。同様にワード線試験時にもワード線の断線などの不良がない限りＷＬ１が選択されるとＸＢＬｄには“Ｌ”レベルの電位、ＢＬｄには“Ｈ”レベルの電位が現れるので“１”データが読み出され、ＷＬ２が選択されるとＸＢＬｄには“Ｈ”レベルの電位、ＢＬｄには“Ｌ”レベルの電位が現れるので“０”データが読み出されることになる。この様に従来の試験方法および半導体記憶装置では最低（ｍ×ｎ）回メモリセルにデータを書き込んだ後、同データを読み出してデータの照合を行わなければならず、簡易試験でもメモリセルに対して最低（２×ｍ×ｎ）回のアクセスが必要になる。これに対して本発明の実施例における半導体記憶装置を用いれば（ｍ＋ｎ）回のアクセスでデータを読み出して照合すればよいため、試験にかかる時間が大幅に短縮され、半導体記憶装置のビット容量が大きい程製造コストの削減に貢献することができる。

【０００７】図４は本発明の一実施例におけるメモリセルアレイの半導体基板のウェル領域のパターンの概略図である。この図は完全ＣＭＯＳ型のメモリセルを使った場合のウェル領域を示しており、空白の領域６はＰチャネル型トランジスタが形成されるＮウェル領域、ハッチの領域７はＮチャネル型トランジスタが形成されるＰウェル領域である。図４ではメモリセルアレイの一部分しか表示していないが最外周のＰウェル領域にダミーのメモリセルが形成され、メモリセルの上辺と右辺を連続して取り囲んでいる。一般に半導体装置の集積度を上げるためにメモリセルアレイ内ではレイアウト・パターンが密になっており、入出力回路などの周辺回路では歩留まり向上の観点からメモリセルアレイに比べて疎になっている。この様な疎密の境界すなわちメモリセルアレイの外周部では、レジストの後退あるいはローディング効果などによりウェル領域が細くなりリークの原因にもなり得る。また、周辺回路が動作したときの電源電圧の揺れがメモリセルに記憶されたデータが破壊されるのを防ぐために、従来からメモリセルアレイの外周にはダミーのメモリセルを含んだガードリングが配置されていた。し

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かし、従来のダミーは単純に形状のみのダミーであり、単に拡散領域が配置された物や、トランジスタが形成されていてもゲート電極を電圧固定したり、ソース・ドレインを浮かせてある物が多かった。また、配置される場所もメモリセルアレイの周囲を取り囲むのではなく、図４に対応させるとメモリセルアレイの上辺のみに配置されることが多かった。しかし、本発明の実施例である図４では従来ダミーのメモリセルを配置していた領域を有効に使っているため半導体チップが大きくなることはない。また、ダミーのメモリセルが周辺回路と隣接するメモリセルアレイの二辺を取り囲み、ダミーのメモリセルのトランジスタを形成するウェル領域を連続して配置できるのでウェル間のリークにも強く、周辺回路からの影響を受けにくいというメリットもある。

【０００８】

【発明の効果】以上説明したようにワード線およびビット線のデコーダから最も遠いメモリセルの外側に内部記憶値が固定されたダミーのメモリセルを配置することにより、半導体記憶装置の試験時にはこの固定されたデータを順次読み込むだけでワード線およびビット線の試験が可能であり、試験時間の短縮、更にはチップコストの低減を図れる効果がある。また、上記のダミーセルを従来の形状ダミーを配置する場所に配置したので、チップ面積が大きくなることもなく、周辺回路からのノイズを受けにくいメモリセルを提供できるという効果もある。

【図面の簡単な説明】

【図１】本発明の実施例におけるメモリセル周辺のブロック図。

【図２】従来のメモリセル周辺のブロック図。

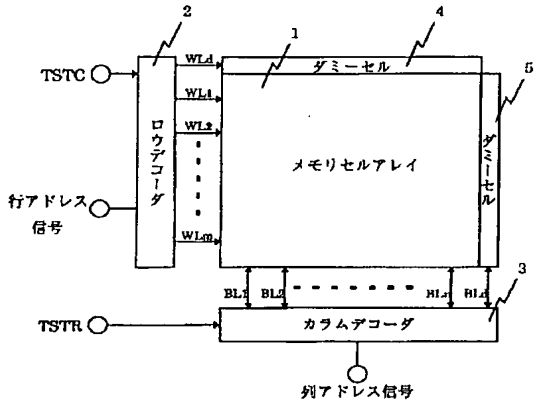
【図３】本発明の実施例におけるダミーのメモリセル近辺の回路図。

【図４】本発明の実施例におけるダミーのメモリセル近辺のウェル配置図。

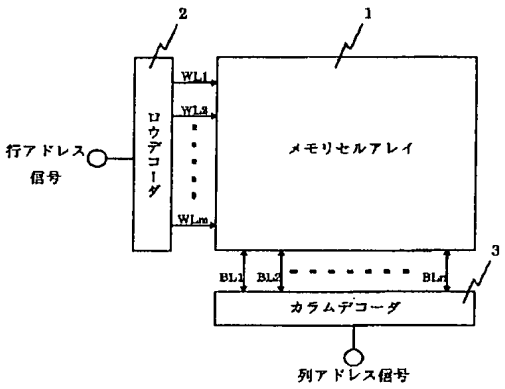
【符号の説明】

１　メモリセルアレイ
２　ロウデコーダ
３　カラムデコーダ
４，５　ダミーセル
１１～１４　完全ＣＭＯＳ型メモリセル
４１～４４，５１～５４　Ｎチャネル型トランジスタ
６　Ｎウェル領域
７　Ｐウェル領域

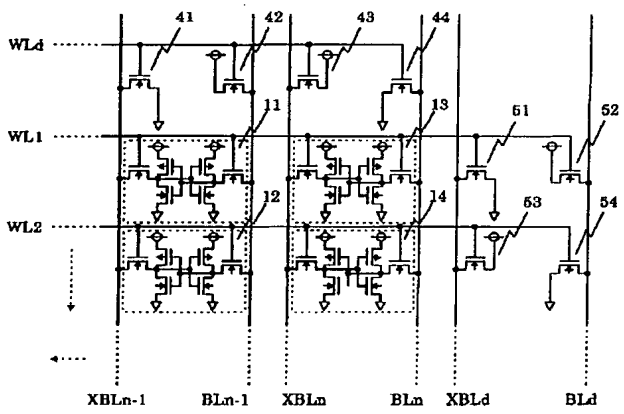
【図１】


TSTC
TSTR
行アドレス信号
ロウデコーダ
ダミーセル
メモリセルアレイ
ダミーセル
カラムデコーダ
列アドレス信号
WLd
WL1
WL2
WLm
BL1
BL2
BLn
BLd
1
2
3
4
5

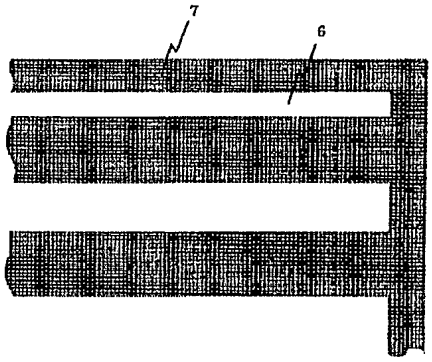
【図２】


行アドレス信号
ロウデコーダ
メモリセルアレイ
カラムデコーダ
列アドレス信号
WL1
WL2
WLm
BL1
BL2
BLn
1
2
3

【図３】


WLd
WL1
WL2
41
42
43
44
11
13
51
52
12
14
53
54
XBLn-1
BLn-1
XBLn
BLn
XBLd
BLd

【図４】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CLAIMS

[Claim(s)]
[Claim 1] The semiconductor memory characterized by providing the memory cell prepared in the crossover part of two or more word lines and the bit line with which the address signal inputted is decoded and chosen from the exterior, and a this each word line and each bit line, and providing the memory cell of the dummy with which the internal-storage value was fixed to the outside of the furthest memory cell from the decoder of the word line of said address signal, and a bit line.
[Claim 2] The memory cell of a dummy according to claim 1 is the semiconductor memory characterized by connecting with the bit line pair of the complementation chosen by the trial means, and connecting with the word line with which the address signal inputted from the outside is decoded and chosen.
[Claim 3] The memory cell of a dummy according to claim 1 is the semiconductor memory characterized by connecting with the word line chosen by the trial means, and connecting with the bit line of the complementation with which the address signal into which a transmission transistor is inputted from the outside is decoded and chosen.
[Claim 4] The source or a drain is connected to the memory cell of said dummy at one bit line. The transmission transistor to which the word line chosen at the time of the word line with which the address signal inputted from the outside is decoded and chosen, or a trial is connected is prepared in the gate. With the terminal connected to the bit line of this transmission transistor, the terminal by the side of reverse is being fixed to the first supply voltage. The semiconductor memory characterized by fixing the terminal by the side of reverse to the second supply voltage with the terminal connected to the bit line of a transmission transistor with the same configuration as another bit line.
[Claim 5] It is the semiconductor memory which the transistor which constitutes the memory cell of said dummy is a single conductivity type, has been arranged to the same well field, and was characterized by this well field enclosing the perimeter of a memory cell array continuously.

[Translation done.]

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DETAILED DESCRIPTION

[Detailed Description of the Invention]
[0001]
[Field of the Invention] Especially this invention relates to the simple trial of a word line and a bit line about a semiconductor memory.
[0002]
[Description of the Prior Art] As the conventional semiconductor memory is shown in the block diagram of the memory cell circumference of drawing 2 , the signal with which the PURIDE code of the address signal inputted from the outside was carried out is inputted into the low decoder 2 as a line address signal, and this low decoder decodes a line address signal further, and chooses one in WLm from m word lines WL1. The column decoder 3 which considered as the input the train address signal to which the PURIDE code of the address signal similarly inputted from the outside on the other hand was carried out chooses one in BLn from n bit lines BL1. Although it may be 2 data lines of 1 set of complementation, since it is easy, one bit line is displayed. The configuration of the circumference of the memory cell of the semiconductor memory shown in drawing 2 is the same also at ROM (Read Only Memory) read-only also at RAM (Random Access Memory) in which writing/read-out is possible. In order to perform the performance test of the semiconductor memory shown in drawing 2 , it is carried out by choosing one bit line (one pair) at the same time it chooses one word line, writing data, and taking collating of a I / O data. Since the written-in data are read and data are collated once, as for the case of ROM, a memory cell array is beginning to read data several mx n times and, as for the case of RAM, that you may collate with expected value only writes in data, it will think simply and about 2 times [of ROM] test time will start. Moreover, since memory space also followed the one way of increase and had to stop also having to spare huge time amount also for the test time of a semiconductor device in connection with it with detailed-izing of a semi-conductor process in recent years, it will lead also to the cost rise of a semiconductor device.
[0003]
[Problem(s) to be Solved by the Invention] The same trial is performed, also after a semiconductor device usually examines to all memory cells in the state of a wafer and is packed by the mold article etc. Test time for that will rebound upon the cost of a semiconductor device directly. Then, although compaction of test time is required, by the conventional approach, it must examine to all memory cells and there is a fault that shortening of test time cannot be attained.
[0004]
[Means for Solving the Problem] It is characterized by providing the memory cell prepared in the crossover part of two or more word lines and the bit line with which the address signal inputted is decoded and chosen from the exterior, and a this each word line and each bit line, and providing the memory cell of the dummy with which the internal-storage value was fixed to the outside of the furthest memory cell from the decoder of the word line of said address signal, and a bit line.
[0005]
[Embodiment of the Invention] Next, this invention is explained with reference to a drawing. Drawing 1

is the block diagram of the memory cell circumference in one example of this invention. The array of the memory cell by which one in drawing has been arranged in the shape of [of a m line n train] a matrix, the low decoder as which 2 chooses a word line, the column decoder as which 3 chooses a bit line, and 4 and 5 are the memory cells of the dummy with which the internal-storage value was fixed. The address signal inputted from the semiconductor device exterior in normal operation is inputted into the back low decoder 2 by which the PURIDE code was carried out if needed as a line address signal through an address input circuit. In response, a low decoder performs decoding actuation further, and chooses only one word line from from among m word lines WL1 to WLm(s). The address signal similarly inputted from the exterior should pass an address input circuit. By being inputted into the back column decoder 3 by which the PURIDE code was carried out if needed as a train address signal, and a column decoder's performing decoding actuation further, and choosing one in BLn (one pair) from n bit lines (n pairs) BL1 The memory cell which exists in the intersection of the selected word line and a bit line becomes active, and read-out and writing are attained to a memory cell. The above actuation is as unchanging as the conventional semiconductor memory. Next, when examining a semi-conductor, and a test signal is inputted from the semiconductor device exterior and a bit line is examined, Stimulus TSTC is inputted into the low decoder 2, and a low decoder starts the word line WLd which forbids decoding actuation of a line address signal and is connected to the dummy cell 4 to the same timing as the usual word line. A train address signal is changed in this condition, sequential selection of the bit line is made, the data of a dummy memory cell are read n times, and it examines by collating with the internal-storage value of the memory cell of the dummy set up beforehand. Since similarly Stimulus TSTR is inputted into the column decoder 3 when examining a word line, a column decoder chooses the bit line BLd which forbids decoding actuation of a train address signal and is connected to the dummy cell 5 to the same timing as the usual bit line. A line address signal is changed in this condition, sequential selection of the word line is made, the data of a dummy memory cell are read m times, and it examines by collating with the internal-storage value of the memory cell of the dummy set up beforehand. Thus, since a simple trial is performed by making the single selection of a word line and the bit line one by one (m+n), the trial of a short time of reading the data of a time dummy cell is attained.

[0006] Drawing 3 shows some circuit diagrams of the memory cell array in drawing 1 , and a dummy cell. The memory cells 11-14 surrounded with the wavy line are memory cells of the perfect CMOS mold which consists of a load transistor which consists of the transmission transistor and drive transistor which consist of two N channel mold transistors each, and two P channel mold transistors. Although the memory cell of a perfect CMOS mold is used by a diagram, the thing whose load transistor is TFT, or the thing of a high resistance mold is also available. 41 to 44 is the N channel mold transistor connected to the word line WLd chosen at the time of the trial of a bit line in the gate, and is the dummy cell by which a drain or the source was connected to bit line pair XBLn-1/BLn-1 and XBLn/BLn of the complementation, and another terminal was connected to power-source potential or touch-down potential. 51 to 54 is the N channel mold transistor connected to the word line chosen at the time of normal operation in the gate, and is the dummy cell by which a drain or the source was connected to bit line pair XBLd/BLnd of the complementation chosen at the time of a trial, and another terminal was connected to power-source potential or touch-down potential. The usual actuation is first explained using drawing 3 . The transmission transistor of the memory cell which it is inputted into the back low decoder to which the PURIDE code of the address signal inputted from the semiconductor device exterior was carried out through the address input circuit if needed as a line address signal, a low decoder performs decoding actuation further in response, the inside of m word lines WL1 to WLm to one word line is chosen, and logical level becomes "H", and is connected to this word line turns on. The address signal similarly inputted from the exterior should pass an address input circuit. By being inputted into the back column decoder by which the PURIDE code was carried out if needed as a train address signal, and a column decoder's performing decoding actuation further, and choosing one pair in XBLn/BLn from n pairs of bit lines XBL1/BL1 The memory cell which exists in the intersection of the selected word line and a bit line becomes active, and read-out and writing are attained to a memory cell. For example, if a word line WL1 and bit line XBLn-1/BLn-1 are chosen, although access becomes

possible to a memory cell 11 and not being displayed on drawing, when reading data, the potential difference of the storage node of a memory cell will appear in a bit line pair through a transmission transistor, and will amplify this very small potential difference with a sense amplifier. "0" data will be held at the memory cell by which potential lower than XBLn-1 appears in BLn-1, and the storage node of the memory cell connected to XBLn-1 through the transmission transistor corresponds to it if the node by the side of "H" level and reverse is "L" level. Conversely, "1" data will be held at the memory cell to which the storage node of the memory cell connected to XBLn-1 through the transmission transistor corresponds if the node by the side of "L" level and reverse is "H" level. The potential which the large potential difference attached from the light buffer connected to the selected bit line at the time of the writing of data is given to a bit line pair, and is written in a memory cell as logical data through a transmission transistor. That is, in writing "0" data in a memory cell, the potential of "L" level is given to "H" level and XBLn-1 BLn-1, and the reverse potential is given to write in "1." The conventional semiconductor memory writes the data of a specific pattern in a memory cell by such actuation at the time of a trial, by reading data from a memory cell, takes collating of data within a testing device, and judges the quality of a semiconductor memory. However, if the memory cell of the dummy of drawing 3 which is one example of this invention is used, it is not necessary to write in data. When examining a bit line first, only the dummy word line WLd is chosen to the same timing as the usual word line, and it rises on "H" level. Next, by changing the train address signal given from the outside, sequential selection of the bit line is made from XBL1/BL1 to XBLn/BLn, the data of a dummy memory cell are read n times, and it examines by collating with the internal-storage value of the memory cell of the dummy set up beforehand. Similarly, when examining a word line, dummy bit line XBLd/BLd is chosen to the same timing as the usual bit line. The line address signal given from the outside in this condition is changed, sequential selection of the word line is made from WL1 to WLm, the data of a dummy memory cell are read m times, and it examines by collating with the internal-storage value of the memory cell of the dummy set up beforehand. namely, the time of a bit line trial -- a bit line -- if sequential selection of XBLn-1/BLn-1 and XBLn/BLn is made unless which short defect can be found -- XBLn-1 -- the potential of "L" level, and BLn-1 -- " -- since the potential of H" level appears, "1" data is read -- XBLn -- the potential of "H" level, and BLn -- "L" -- since the potential of level appears, "0" data will be read. Since the potential of "L" level will appear in the potential of "H" level, and BLd at XBLd if "1" data is read and WL2 is chosen, since the potential of "H" level will appear in the potential of "L" level, and BLd at XBLd if WL1 is chosen as long as there are no defects, such as an open circuit of a word line, similarly also at the time of a word line trial, "0" data will be read. Thus, in a conventional test method and a conventional semiconductor memory, after writing data in the minimum (mxn) time memory cell, these data must be read, data must be collated and access of the minimum (2xmxn) time is [as opposed to / in a simple trial / a memory cell] needed. On the other hand, since what is necessary is to read data and just to collate by access of a time, if the semiconductor memory in the example of this invention is used (m+n), the time amount concerning a trial is shortened sharply, and it can contribute to reduction of a manufacturing cost, so that the bit capacity of a semiconductor memory is large.

[0007] Drawing 4 is the schematic diagram of the pattern of the well field of the semi-conductor substrate of the memory cell array in one example of this invention. This drawing shows the well field at the time of using the memory cell of a perfect CMOS mold, and, as for the field 6 of a null, the N channel mold transistor of N well field in which a P channel mold transistor is formed, and the field 7 of a hatch way is P well field formed. In drawing 4 , although a part of memory cell array is displayed, a dummy memory cell is formed in P well field of the outermost periphery, and the surface and the right-hand side of a memory cell are surrounded continuously. In order to raise the degree of integration of a semiconductor device generally, within the memory cell array, the layout pattern is dense and has become a non-dense from a viewpoint of the improvement in the yield compared with the memory cell array in circumference circuits, such as an I/O circuit. A well field becomes thin according to retreat or a loading effect of a resist etc., and it can also become the cause of leak, such the boundary of roughness and fineness, i.e., the periphery section of a memory cell array. Moreover, in order to prevent destroying the data with which the shake of supply voltage when a circumference circuit operates was memorized

by the memory cell, the guard ring containing a dummy memory cell is arranged from the former at the periphery of a memory cell array. However, the conventional dummy was a dummy of only a configuration simply and there were many objects with which the diffusion field has only been arranged, and objects which carry out the voltage clamp of the gate electrode even if the transistor is formed, or have floated the source drain. Moreover, if the location arranged does not enclose the perimeter of a MEMORIZERU array, either but was made to correspond to drawing 4 , it will have been arranged only at the surface of a memory cell array in many cases. However, in drawing 4 which is the example of this invention, since the field which arranged the dummy memory cell conventionally is used effectively, a semiconductor chip does not become large. Moreover, two sides of the memory cell array by which a dummy memory cell adjoins a circumference circuit are surrounded, and there is also a merit of it being strong also to leak between wells since the well field which forms the transistor of a dummy memory cell can be arranged continuously, and being hard to be influenced from a circumference circuit.

[0008]

[Effect of the Invention] As explained above, the trial of a word line and a bit line is possible only by reading this fixed data one by one at the time of the trial of a semiconductor memory by arranging the memory cell of the dummy with which the internal-storage value was fixed to the outside of the furthest memory cell from the decoder of a word line and a bit line, and there are compaction of test time and effectiveness that reduction of chip cost can be aimed at further. Moreover, it is effective in the ability to offer the memory cell which cannot receive the noise from a circumference circuit easily, without a chip area becoming large since the above-mentioned dummy cell has been arranged in the location which arranges the conventional configuration dummy.

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TECHNICAL FIELD

[Field of the Invention] Especially this invention relates to the simple trial of a word line and a bit line about a semiconductor memory.

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PRIOR ART

[Description of the Prior Art] As the conventional semiconductor memory is shown in the block diagram of the memory cell circumference of drawing 2 , the signal with which the PURIDE code of the address signal inputted from the outside was carried out is inputted into the low decoder 2 as a line address signal, and this low decoder decodes a line address signal further, and chooses one in WLm from m word lines WL1. The column decoder 3 which considered as the input the train address signal to which the PURIDE code of the address signal similarly inputted from the outside on the other hand was carried out chooses one in BLn from n bit lines BL1. Although it may be 2 data lines of 1 set of complementation, since it is easy, one bit line is displayed. The configuration of the circumference of the memory cell of the semiconductor memory shown in drawing 2 is the same also at ROM (Read Only Memory) read-only also at RAM (Random Access Memory) in which writing/read-out is possible. In order to perform the performance test of the semiconductor memory shown in drawing 2 , it is carried out by choosing one bit line (one pair) at the same time it chooses one word line, writing data, and taking collating of a I / O data. Since the written-in data are read and data are collated once, as for the case of ROM, a memory cell array is beginning to read data several mx n times and, as for the case of RAM, that you may collate with expected value only writes in data, it will think simply and about 2 times [of ROM] test time will start. Moreover, since memory space also followed the one way of increase and had to stop also having to spare huge time amount also for the test time of a semiconductor device in connection with it with detailed-izing of a semi-conductor process in recent years, it will lead also to the cost rise of a semiconductor device.

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EFFECT OF THE INVENTION

[Effect of the Invention] As explained above, the trial of a word line and a bit line is possible only by reading this fixed data one by one at the time of the trial of a semiconductor memory by arranging the memory cell of the dummy with which the internal-storage value was fixed to the outside of the furthest memory cell from the decoder of a word line and a bit line, and there are compaction of test time and effectiveness that reduction of chip cost can be aimed at further. Moreover, it is effective in the ability to offer the memory cell which cannot receive the noise from a circumference circuit easily, without a chip area becoming large since the above-mentioned dummy cell has been arranged in the location which arranges the conventional configuration dummy.

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TECHNICAL PROBLEM

[Problem(s) to be Solved by the Invention] The same trial is performed, also after a semiconductor device usually examines to all memory cells in the state of a wafer and is packed by the mold article etc. Test time for that will rebound upon the cost of a semiconductor device directly. Then, although compaction of test time is required, by the conventional approach, it must examine to all memory cells and there is a fault that shortening of test time cannot be attained.

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MEANS

[Means for Solving the Problem] It is characterized by providing the memory cell prepared in the crossover part of two or more word lines and the bit line with which the address signal inputted is decoded and chosen from the exterior, and a this each word line and each bit line, and providing the memory cell of the dummy with which the internal-storage value was fixed to the outside of the furthest memory cell from the decoder of the word line of said address signal, and a bit line.
[0005]
[Embodiment of the Invention] Next, this invention is explained with reference to a drawing. Drawing 1 is the block diagram of the memory cell circumference in one example of this invention. The array of the memory cell by which one in drawing has been arranged in the shape of [of a m line n train] a matrix, the low decoder as which 2 chooses a word line, the column decoder as which 3 chooses a bit line, and 4 and 5 are the memory cells of the dummy with which the internal-storage value was fixed. The address signal inputted from the semiconductor device exterior in normal operation is inputted into the back low decoder 2 by which the PURIDE code was carried out if needed as a line address signal through an address input circuit. In response, a low decoder performs decoding actuation further, and chooses only one word line from from among m word lines WL1 to WLm(s). The address signal similarly inputted from the exterior should pass an address input circuit. By being inputted into the back column decoder 3 by which the PURIDE code was carried out if needed as a train address signal, and a column decoder's performing decoding actuation further, and choosing one in BLn (one pair) from n bit lines (n pairs) BL1 The memory cell which exists in the intersection of the selected word line and a bit line becomes active, and read-out and writing are attained to a memory cell. The above actuation is as unchanging as the conventional semiconductor memory. Next, when examining a semi-conductor, and a test signal is inputted from the semiconductor device exterior and a bit line is examined, Stimulus TSTC is inputted into the low decoder 2, and a low decoder starts the word line WLd which forbids decoding actuation of a line address signal and is connected to the dummy cell 4 to the same timing as the usual word line. A train address signal is changed in this condition, sequential selection of the bit line is made, the data of a dummy memory cell are read n times, and it examines by collating with the internal-storage value of the memory cell of the dummy set up beforehand. Since similarly Stimulus TSTR is inputted into the column decoder 3 when examining a word line, a column decoder chooses the bit line BLd which forbids decoding actuation of a train address signal and is connected to the dummy cell 5 to the same timing as the usual bit line. A line address signal is changed in this condition, sequential selection of the word line is made, the data of a dummy memory cell are read m times, and it examines by collating with the internal-storage value of the memory cell of the dummy set up beforehand. Thus, since a simple trial is performed by making the single selection of a word line and the bit line one by one (m+n), the trial of a short time of reading the data of a time dummy cell is attained.
[0006] Drawing 3 shows some circuit diagrams of the memory cell array in drawing 1 , and a dummy cell. The memory cells 11-14 surrounded with the wavy line are memory cells of the perfect CMOS mold which consists of a load transistor which consists of the transmission transistor and drive transistor which consist of two N channel mold transistors each, and two P channel mold transistors. Although the

memory cell of a perfect CMOS mold is used by a diagram, the thing whose load transistor is TFT, or the thing of a high resistance mold is also available. 41 to 44 is the N channel mold transistor connected to the word line WLd chosen at the time of the trial of a bit line in the gate, and is the dummy cell by which a drain or the source was connected to bit line pair XBLn-1/BLn-1 and XBLn/BLn of the complementation, and another terminal was connected to power-source potential or touch-down potential. 51 to 54 is the N channel mold transistor connected to the word line chosen at the time of normal operation in the gate, and is the dummy cell by which a drain or the source was connected to bit line pair XBLd/BLnd of the complementation chosen at the time of a trial, and another terminal was connected to power-source potential or touch-down potential. The usual actuation is first explained using drawing 3 . The transmission transistor of the memory cell which it is inputted into the back low decoder to which the PURIDE code of the address signal inputted from the semiconductor device exterior was carried out through the address input circuit if needed as a line address signal, a low decoder performs decoding actuation further in response, the inside of m word lines WL1 to WLm to one word line is chosen, and logical level becomes "H", and is connected to this word line turns on. The address signal similarly inputted from the exterior should pass an address input circuit. By being inputted into the back column decoder by which the PURIDE code was carried out if needed as a train address signal, and a column decoder's performing decoding actuation further, and choosing one pair in XBLn/BLn from n pairs of bit lines XBL1/BL1 The memory cell which exists in the intersection of the selected word line and a bit line becomes active, and read-out and writing are attained to a memory cell. For example, if a word line WL1 and bit line XBLn-1/BLn-1 are chosen, although access becomes possible to a memory cell 11 and not being displayed on drawing, when reading data, the potential difference of the storage node of a memory cell will appear in a bit line pair through a transmission transistor, and will amplify this very small potential difference with a sense amplifier. "0" data will be held at the memory cell by which potential lower than XBLn-1 appears in BLn-1, and the storage node of the memory cell connected to XBLn-1 through the transmission transistor corresponds to it if the node by the side of "H" level and reverse is "L" level. Conversely, "1" data will be held at the memory cell to which the storage node of the memory cell connected to XBLn-1 through the transmission transistor corresponds if the node by the side of "L" level and reverse is "H" level. The potential which the large potential difference attached from the light buffer connected to the selected bit line at the time of the writing of data is given to a bit line pair, and is written in a memory cell as logical data through a transmission transistor. That is, in writing "0" data in a memory cell, the potential of "L" level is given to "H" level and XBLn-1 BLn-1, and the reverse potential is given to write in "1." The conventional semiconductor memory writes the data of a specific pattern in a memory cell by such actuation at the time of a trial, by reading data from a memory cell, takes collating of data within a testing device, and judges the quality of a semiconductor memory. However, if the memory cell of the dummy of drawing 3 which is one example of this invention is used, it is not necessary to write in data. When examining a bit line first, only the dummy word line WLd is chosen to the same timing as the usual word line, and it rises on "H" level. Next, by changing the train address signal given from the outside, sequential selection of the bit line is made from XBL1/BL1 to XBLn/BLn, the data of a dummy memory cell are read n times, and it examines by collating with the internal-storage value of the memory cell of the dummy set up beforehand. Similarly, when examining a word line, dummy bit line XBLd/BLd is chosen to the same timing as the usual bit line. The line address signal given from the outside in this condition is changed, sequential selection of the word line is made from WL1 to WLm, the data of a dummy memory cell are read m times, and it examines by collating with the internal-storage value of the memory cell of the dummy set up beforehand. namely, the time of a bit line trial -- a bit line -- if sequential selection of XBLn-1/BLn-1 and XBLn/BLn is made unless which short defect can be found -- XBLn-1 -- the potential of "L" level, and BLn-1 -- " -- since the potential of H" level appears, "1" data is read -- XBLn -- the potential of "H" level, and BLn -- "L" -- since the potential of level appears, "0" data will be read. Since the potential of "L" level will appear in the potential of "H" level, and BLd at XBLd if "1" data is read and WL2 is chosen, since the potential of "H" level will appear in the potential of "L" level, and BLd at XBLd if WL1 is chosen as long as there are no defects, such as an open circuit of a

word line, similarly also at the time of a word line trial, "0" data will be read. Thus, in a conventional test method and a conventional semiconductor memory, after writing data in the minimum (mxn) time memory cell, these data must be read, data must be collated and access of the minimum (2xmxn) time is [as opposed to / in a simple trial / a memory cell] needed. On the other hand, since what is necessary is to read data and just to collate by access of a time, if the semiconductor memory in the example of this invention is used (m+n), the time amount concerning a trial is shortened sharply, and it can contribute to reduction of a manufacturing cost, so that the bit capacity of a semiconductor memory is large.

[0007] Drawing 4 is the schematic diagram of the pattern of the well field of the semi-conductor substrate of the memory cell array in one example of this invention. This drawing shows the well field at the time of using the memory cell of a perfect CMOS mold, and, as for the field 6 of a null, the N channel mold transistor of N well field in which a P channel mold transistor is formed, and the field 7 of a hatch way is P well field formed. In drawing 4 , although a part of memory cell array is displayed, a dummy memory cell is formed in P well field of the outermost periphery, and the surface and the right-hand side of a memory cell are surrounded continuously. In order to raise the degree of integration of a semiconductor device generally, within the memory cell array, the layout pattern is dense and has become a non-dense from a viewpoint of the improvement in the yield compared with the memory cell array in circumference circuits, such as an I/O circuit. A well field becomes thin according to retreat or a loading effect of a resist etc., and it can also become the cause of leak, such the boundary of roughness and fineness, i.e., the periphery section of a memory cell array. Moreover, in order to prevent destroying the data with which the shake of supply voltage when a circumference circuit operates was memorized by the memory cell, the guard ring containing a dummy memory cell is arranged from the former at the periphery of a memory cell array. However, the conventional dummy was a dummy of only a configuration simply and there were many objects with which the diffusion field has only been arranged, and objects which carry out the voltage clamp of the gate electrode even if the transistor is formed, or have floated the source drain. Moreover, if the location arranged does not enclose the perimeter of a MEMORIZERU array, either but was made to correspond to drawing 4 , it will have been arranged only at the surface of a memory cell array in many cases. However, in drawing 4 which is the example of this invention, since the field which arranged the dummy memory cell conventionally is used effectively, a semiconductor chip does not become large. Moreover, two sides of the memory cell array by which a dummy memory cell adjoins a circumference circuit are surrounded, and there is also a merit of it being strong also to leak between wells since the well field which forms the transistor of a dummy memory cell can be arranged continuously, and being hard to be influenced from a circumference circuit.

[Translation done.]

DESCRIPTION OF DRAWINGS

[Brief Description of the Drawings]
[Drawing 1] The block diagram of the memory cell circumference in the example of this invention.
[Drawing 2] The conventional block diagram of the memory cell circumference.
[Drawing 3] The circuit diagram of the memory cell neighborhood of the dummy in the example of this invention.
[Drawing 4] The well plot plan of the memory cell neighborhood of the dummy in the example of this invention.
[Description of Notations]
1 Memory Cell Array
2 Low Decoder
3 Column Decoder
4 Five Dummy cell
11-14 Perfect CMOS mold memory cell
41-44, 51-54 N channel mold transistor
6 N Well Field
7 P Well Field

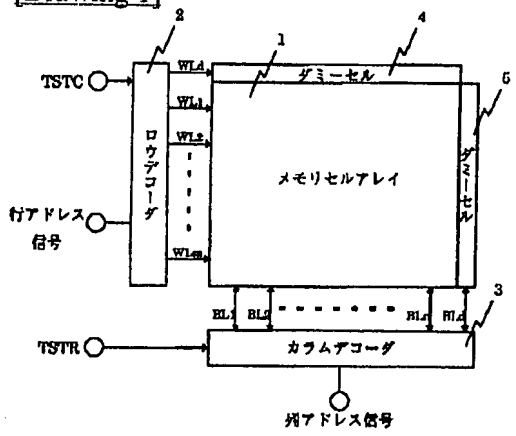
[Translation done.]

* NOTICES *

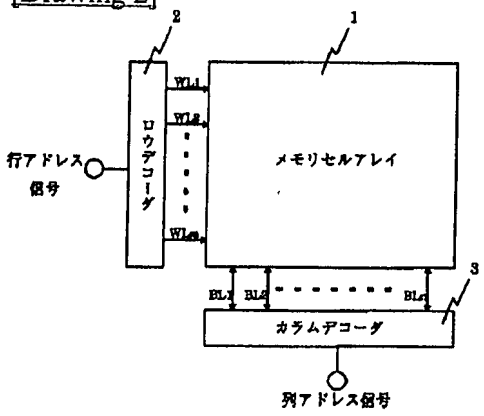
1.This document has been translated by computer. So the translation may not reflect the original precisely.
2.**** shows the word which can not be translated.
3.In the drawings, any words are not translated.

DRAWINGS

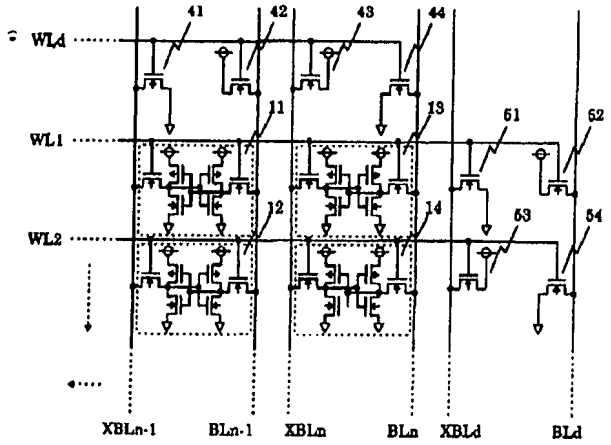
[Drawing 1]



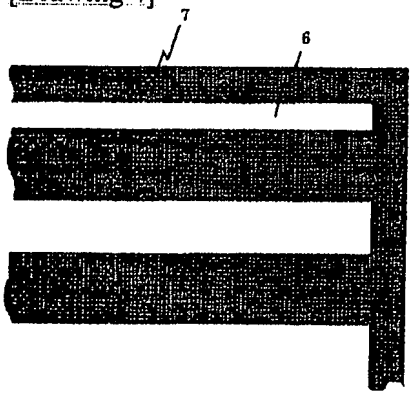
[Drawing 2]



[Drawing 3]



[Drawing 4]



[Translation done.]